REMARKS/ARGUMENTS

Claims 1-23 are currently pending in this application. Claims 1-23 were rejected in the subject Office Action. Claims 1, 18 and 21 are hereby amended and Applicants respectfully request re-examination, reconsideration and allowance of each of pending claims 1-23.

I. Claim Rejections – 35 U.S.C. § 102

On page 2 of the subject Office Action, claims 1-2, 6 and 12-13 were rejected under 35 U.S.C. § 102(b) as being anticipated by Matsuda *et al.* (U.S. Patent Publication No. 2002/0000379), hereinafter "Matsuda". Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

Claim 1 is an independent claim and each of claims 2, 6 and 12-13 depend, directly or indirectly, from amended independent claim 1. Independent claim 1 recites the feature of:

immersing the wafer in an electrolytic solution.

Matsuda does not teach immersing the wafer in an electrolytic solution. Rather, Matsuda is directed to using a technique in which only one side of the wafer contacts the solution. Applicants submit that it is well known that to immerse means to completely surround or completely envelope or to be inserted into. Each of the figures of Matsuda that show a substrate, namely FIGS. 1, 4, 5, 8A, 8B, 9A and 9B, clearly show that the wafer 101, 204 is NOT immersed in the electrolyte solution. Rather, a technique called "liquid contact" is used to avoid bubble formation on the surface. In each case, only one side of the wafer is in contact with the electroplating solution with the other side in contact with a wafer holder which serves as a dummy cathode. Paragraph [0065] of Matsuda describes the "liquid contact" technique and in no case is the wafer immersed in the electroplating solution. Rather, it is simply subjacently contacted by the solution. Because of Matsuda's dissertation on the advantage of

"liquid contact", Applicants respectfully submit that Matsuda *teaches away* from immersing. At any rate, Matsuda does not teach or suggest immersing.

Since claim 1 recites the feature of immersing the wafer in an electrolyte solution and since dependent claims 2, 6 and 12-13 recite the same by way of incorporation, each of claims 1-2, 6 and 12-13 is distinguished from Matsuda and the rejection of these claims under 35 U.S.C. § 102(b), should be withdrawn.

II. Claim Rejections Under 35 U.S.C. § 103

In the subject Office Action, in particular on page 4, claims 1-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Uzoh *et al.* (U.S. Patent Publication No. 2005/0095854), hereinafter "Uzoh", in view of Matsuda. Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

Claims 1, 18 and 21 are the independent claims of the rejected claim set. Each of these claims has been amended and, as amended, each is directed to electroplating (or electrochemically depositing – claim 18) a metal layer on a wafer using a series of steps of different electroplating conditions.

Each of claims 1, 18 and 21 generally recite the feature that the first and initial step in the electroplating operation sequence is followed by a second step and the second step includes a

> "second current density being greater than zero and less than the first current density".

Neither of the references show this feature. In **Uzoh**, in each case, i. e. in FIGS. 13-18 of Uzoh, the initial step of the electroplating sequence includes a current density of I_i that is lower than the current density in the next step. Uzoh therefore does not teach the claimed features that are recited in independent claims 1, 18 and 21.

Matsuda also does not teach continuously electroplating a metal layer on a wafer using a series of electroplating steps in which the second step includes a lower current

density than the first and initial step. The timing charts 7A-7G of Matsuda do not represent a continuous electroplating operation used to form a metal film on a wafer; rather, they represent a plating sequence illustrating successive plating operations for plating more than one wafer. As pointed out in paragraph [0049] of Matsuda, with respect to FIGS. 7A-7G.

> "The anode current density (I_{an}) during wafer (cathode) plating and the anode current density (I_{an}) during anode burn-in using the dummy cathode are plotted on the same timing chart for the sake of convenience. "First plating" is for one arbitrary way for a single wafer plating, and "second plating" is for the next wafer. "Interval" is the time between the first and second plating processes".

Moreover, in the only instances among FIGS. 7A-7G that do include a non-zero current during the interval period, namely in FIGS. 7D-7G, this current density is provided to a dummy cathode, i.e., not wafer 1 or 2. This is described in paragraphs [0051] - [0057] and paragraph [0058] which explains that the wafer is not plated during this interval period and recites that " electricity was supplied five or two minutes before plating was resumed because . . .".

Matsuda therefore does not disclose a process sequence for depositing a metal layer on a wafer, much less a sequence for depositing a metal layer on a wafer including a second electroplating step using the current density less than the first electroplating step.

Therefore, each of claims 1 and 21 which recite a continuous electroplating operation and for depositing a metal layer on a wafer, using a plurality of steps, including a second step following the first step and including a lower current density, is distingulshed from the references. Independent claim 18 also recites a method of electrochemically depositing a metal layer on a wafer using a sequence of plating steps with the second step using a lower current density than the first step and is similarly distinguished. Dependent claims 2-17, 19, 20 and 22-23 are distinguished by reason of their dependency.

It is **because** of the feature of an initial high current density electroplating step followed by a second step having a non-zero current density less that that of the first step, that the invention provides the advantage that openings such as vias, even those with high aspect ratios, are completely filled, void-free and include a low contact resistance as discussed in paragraph [0019].

For reasons set forth above, the rejection claims 1-23 under 35 U.S.C. § 103(a) as being unpatentable over Uzoh in view of Matsuda, should be withdrawn.

CONCLUSION

Based on the foregoing, each of pending claims 1-23 is in allowable form and the application in condition for allowance, which action is respectfully and expeditiously requested.

The Assistant Commissioner for Patents is hereby authorized to charge any fees or credit any excess payment that may be associated with this communication to Deposit Account 04-1679.

Respectfully submitted,

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